AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising a clock doubler circuit, the clock doubler circuit comprising:

an input clock terminal;

an output clock terminal;

a first counter circuit having a clock terminal coupled to the input clock terminal and a plurality of output terminals;

a divide-by-two register having a plurality of data input terminals coupled to the output terminals of the first counter circuit, a clock terminal coupled to the input clock terminal, and a plurality of output terminals;

a second counter circuit having a clock terminal coupled to ~~the input clock terminal~~ receive a clock update signal from the first counter circuit, a plurality of data input terminals coupled to the output terminals of the divide-by-two register, and a plurality of output terminals; and

an output clock generator having a plurality of input terminals coupled to the output terminals of the second counter circuit and an output terminal coupled to the output clock terminal of the clock doubler circuit.

2. (Original) The system of Claim 1, wherein the first counter circuit comprises:

a first oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal; and

a first counter having an input terminal coupled to the output terminal of the first oscillator circuit and further having a plurality of output terminals coupled to the data input terminals of the divide-by-two register.

3. (Original) The system of Claim 2, wherein the second counter circuit comprises:

a second oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal, the second oscillator circuit being implemented to oscillate with the same frequency as the first oscillator circuit;

a second counter having an input terminal coupled to the output terminal of the second oscillator circuit and further having a plurality of output terminals;

a first pulse generator circuit having a first set of input terminals coupled to the output terminals of the second counter and an output terminal coupled to a first one of the input terminals of the output clock generator; and

a second pulse generator circuit having a first set of input terminals coupled to the output terminals of the second counter, a second set of input terminals coupled to the output terminals of the divide-by-two register, and an output terminal coupled to a second one of the input terminals of the output clock generator.

4. (Original) The system of Claim 3, wherein the second pulse generator circuit comprises a comparator.

5. (Original) The system of Claim 3, wherein the first pulse generator circuit comprises a comparator, the first pulse generator circuit further having a second set of input terminals each of which is coupled to one of power and ground.

6. (Original) The system of Claim 3, wherein the first pulse generator circuit comprises:

a logical OR gate having input terminals coupled to the output terminals of the second counter and further having an output terminal;

a pass transistor coupled between the input clock terminal and the output terminal of the first pulse generator circuit, the pass transistor having a gate terminal coupled to the output terminal of the logical OR gate; and

a pull-down coupled to the output terminal of the first pulse generator circuit, the pull-down having a gate terminal coupled to the output terminal of the logical OR gate.

7. (Original) The system of Claim 1, wherein the clock doubler circuit further comprises a reset input terminal coupled to reset input terminals of the first counter circuit, the divide-by-two register, and the second counter circuit.

8. (Original) The system of Claim 1, wherein the clock doubler circuit further comprises:

a reset input terminal; and

a flip-flop having a data input terminal coupled to the reset input terminal, a set terminal coupled to the data input terminal, a clock terminal coupled to the input clock terminal of the clock doubler circuit, and an output terminal coupled to reset input terminals of the first counter circuit, the register, and the second counter circuit.

9. (Original) The system of Claim 1, wherein the first counter circuit comprises means for resetting itself after each M input clock periods, wherein M is an integer.

10. (Original) The system of Claim 9, wherein M is five.

11. (Original) The system of Claim 1, wherein the system comprises a programmable logic device (PLD), and the clock doubler circuit is implemented using programmable logic of the PLD.

12. (Original) The system of Claim 11, wherein the PLD is a field programmable gate array (FPGA).

13. (Original) The system of Claim 1, wherein the output clock generator comprises a logical OR circuit having input terminals coupled to the output terminals of the second counter circuit, and further having an output terminal coupled to the output clock terminal of the clock doubler circuit.

14. (Original) A system providing from an input clock signal an output clock signal having a frequency twice that of the input clock signal, the system comprising:

means for counting a first number of counts between successive first edges of the input clock signal;

means for dividing the first number to provide a divided number;

means for counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided number;

means for providing a first pulse on a first signal in response to each first edge of the input clock signal;

means for providing a second pulse on a second signal based on results of comparing the second number with the divided-by-two number; and

means for providing a pulse on the output clock signal whenever a pulse is provided on one of the first and second signals.

15. (Original) The system of Claim 14, further comprising means for repeating the counting the first number of counts and the dividing the first number to provide a divided number every M periods of the input clock signal, wherein M is an integer.

16. (Original) The system of Claim 15, wherein M is five.

17. (Original) The system of Claim 14, wherein the system is implemented using a programmable logic device (PLD).

18. (Original) The system of Claim 17, wherein the PLD is a field programmable gate array (FPGA).

19. (Original) The system of Claim 14, wherein:

the first number has 2 to the power of K possible values, K being an integer;

the divided number has 2 to the power of (K-1) possible values; and

the second number has 2 to the power of (K-1) possible values.

20. (Original) The system of Claim 19, wherein K is eight.

21. (Original) The system of Claim 14, wherein the first edges are rising edges.

22. (Original) The system of Claim 14, wherein the means for dividing the first number comprises means for dividing the first number by two.

23. (Original) A method of providing from an input clock signal an output clock signal having a frequency twice that of the input clock signal, the method comprising:

counting a first number of counts between successive first edges of the input clock signal;

dividing the first number to provide a divided number;

counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided number;

providing a first pulse on a first signal in response to each first edge of the input clock signal;

providing a second pulse on a second signal based on results of comparing the second number with the divided-by-two number; and

providing a pulse on the output clock signal whenever a pulse is provided on one of the first and second signals.

24. (Original) The method of Claim 23, wherein the counting the first number of counts and the dividing the first number to provide a divided number are repeated every M periods of the input clock signal, wherein M is an integer.

25. (Original) The method of Claim 24, wherein M is five.

26. (Original) The method of Claim 23, wherein the steps of the method are performed by a circuit implemented in a programmable logic device (PLD).

27. (Original) The method of Claim 26, wherein the PLD is a field programmable gate array (FPGA).

28. (Original) The method of Claim 27, wherein:

the first number has 2 to the power of K possible values, K being an integer;

the divided number has 2 to the power of (K-1) possible values; and

the second number has 2 to the power of (K-1) possible values.

29. (Original) The method of Claim 28, wherein K is eight.

30. (Original) The method of Claim 23, wherein the first edges are rising edges.

31. (Original) The method of Claim 23, wherein dividing the first number comprises dividing the first number by two.